

REMARKS

Applicants appreciate the detailed examination evidenced by the Official Action mailed September 11, 2008 (hereinafter the Final Official Action). In response, Applicants have significantly amended independent Claim 1 as reflected above to further clarify that embodiments of programming an electronic device can include "transferring command information to the programmable memory controller circuit, wherein command information is used to generate control signals used in conjunction with data information and address information transferred to the buffer circuit, wherein the control signals are generated by the programmable memory controller circuit," which is not disclosed or suggested (either singularly in combination) by the cited references. *Independent Claim 20 includes analogous recitations.* Accordingly, Applicants respectfully request the withdrawal of all rejections and the allowance of all claims for at least the reasons described herein.

Amended Independent Claim 1 is Patentable Over the Cited References

Claims 1, 3, 5, 7, 20, 24, and 27-28 stand rejected under 35 U.S.C. section 103(a) over Ahn in view of Tsai and further in view of Lawman. *Official Action, page 2.* In response, Applicants have amended independent Claim 1 as described above, which highlights, at least, that Tsai does not disclose or suggest the recitation of "transferring command information to the programmable memory controller circuit, wherein command information is used to generate control signals used in conjunction with data information and address information transferred to the buffer circuit, wherein the control signals are generated by the programmable memory controller circuit." as alleged.

As further illustration, Applicants submit that operations of the Memory Controller Circuit 240 shown, for example, in Figure 2 of the present Specification provide that the Memory Controller Circuit 240 only receives command information (not data) from the decoder circuit 230 and generates control signals used in conjunction with data information and address information stored in the buffer circuit 235 (See, for example, the present Specification at page 9, line 30 to page 10, line 14 providing exemplary illustration of some of the operations of the Memory Controller Circuit 240 and other circuits). Further, the

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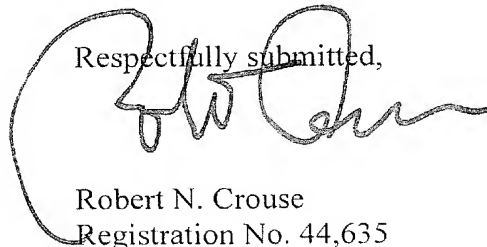
decoder circuit 230 transfers data information and address information included in the program data to the buffer circuit 235 and command information included in the program data to the programmable memory controller circuit 240.

In contrast to operations of the Memory Controller Circuit 240 and the recitations of independent Claim 1, Figure 3 and the associated discussion at column 7, lines 14-40 in Tsai teach that the programming controller 32 receives instructions and data from the IE bus 10.

Further, Tsai and Ahn do not disclose or suggest (either singularly in combination) the buffer circuit 235 that stores data information and address information included in the program data both when the programmable memory controller circuit 240 operates and when the general operation processor circuit 210 operates. Further, Lawman does not disclose or suggestion the recitations shown above to be missing from Tsai and Ahn. Therefore, even if the cited references were combined, the combination would not disclose or suggest at least the recitations of amended independent Claim 1 and independent Claim 20 described above, as required under section 103. Furthermore, the dependent claims are patentable at least per the patentability of amended independent Claim 1 and independent Claim 20.

Applicants respectfully request entry of the present Amendment and the allowance of all claims in due course for at least the reasons described herein. If any informal matters arise the Examiner is encouraged to telephone the undersigned at 919-854-1400 for resolution of any outstanding issues.

Respectfully submitted,



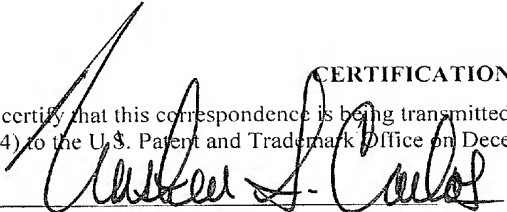
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